

100

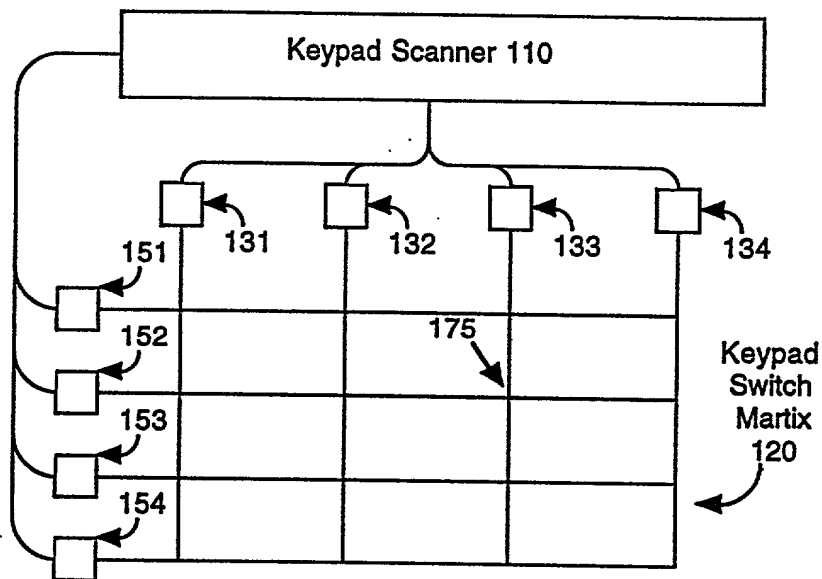


FIG 1 A

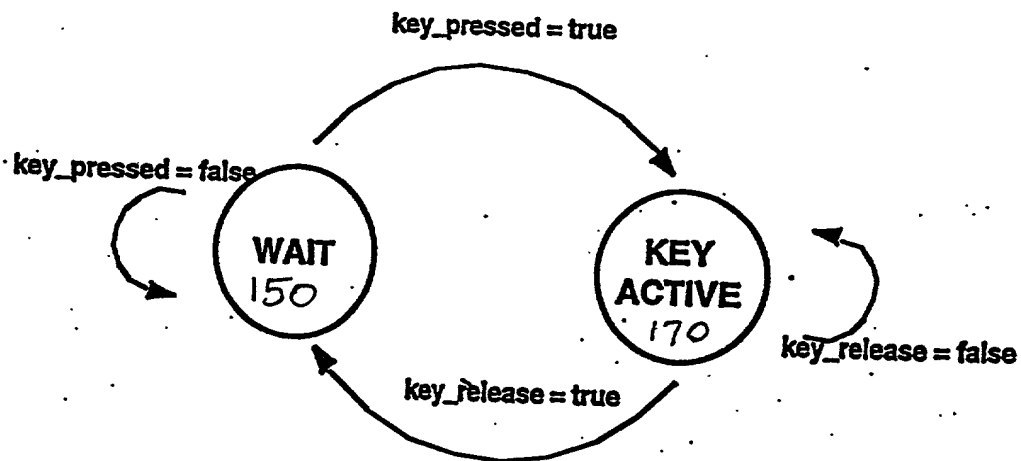


FIG 1 B

200

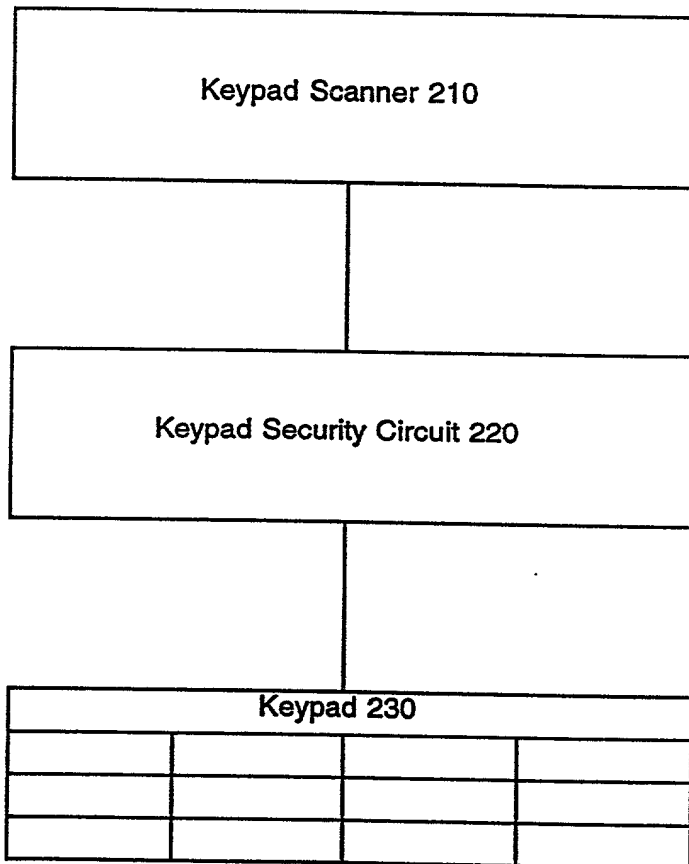


FIG 2

300

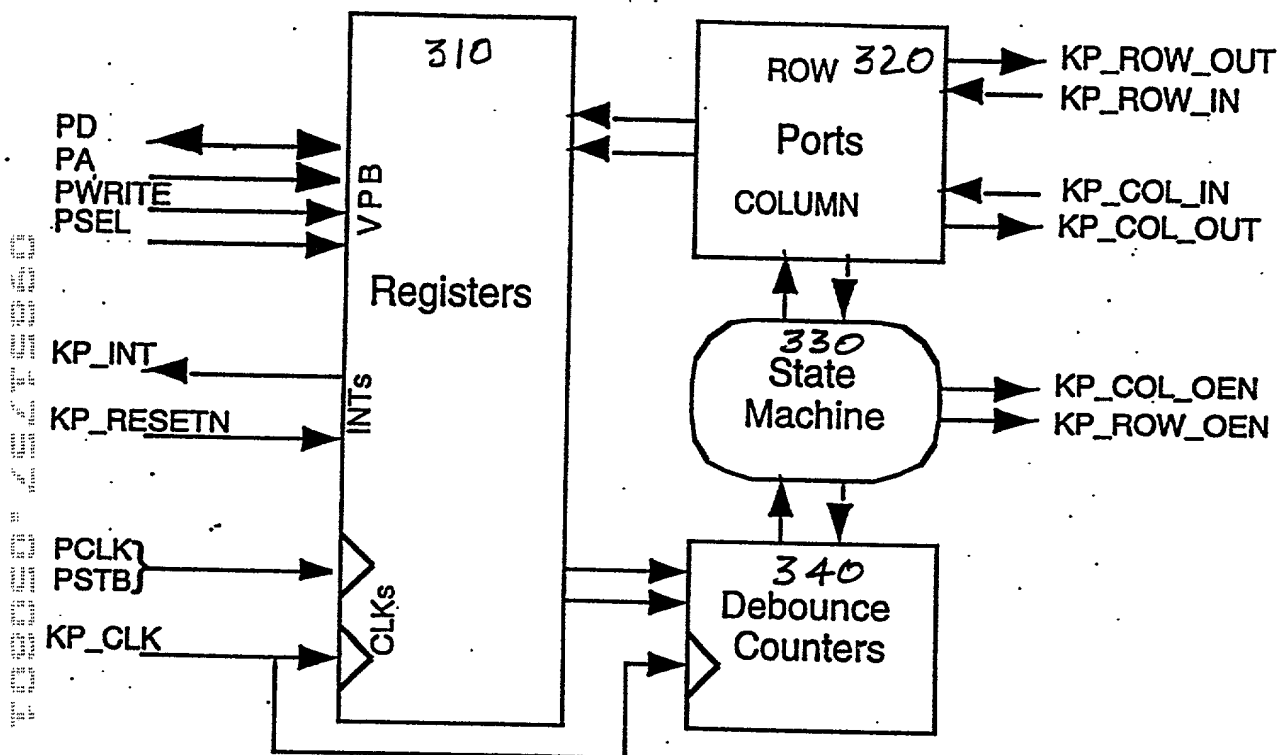


Fig 3

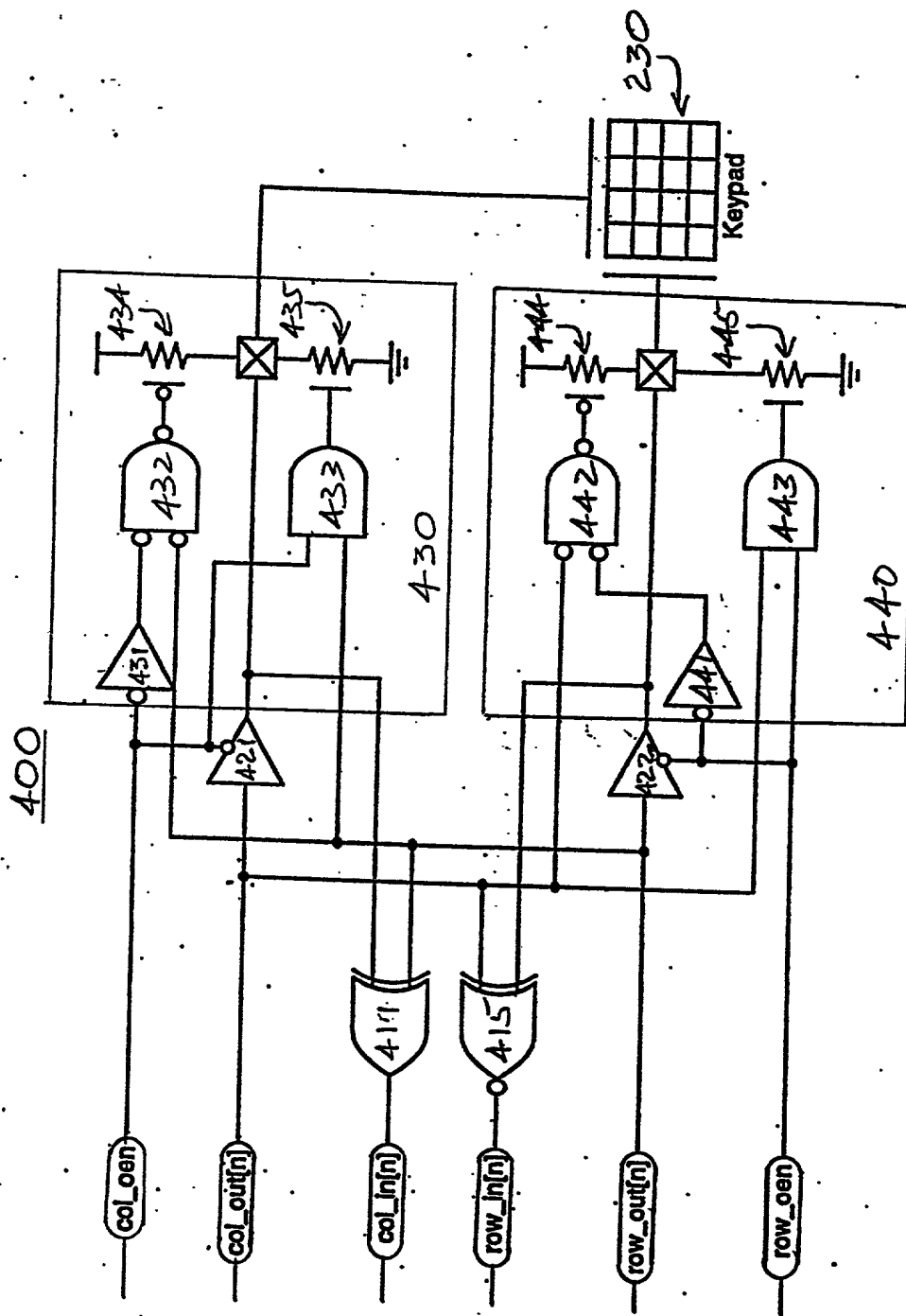


Fig 4

500

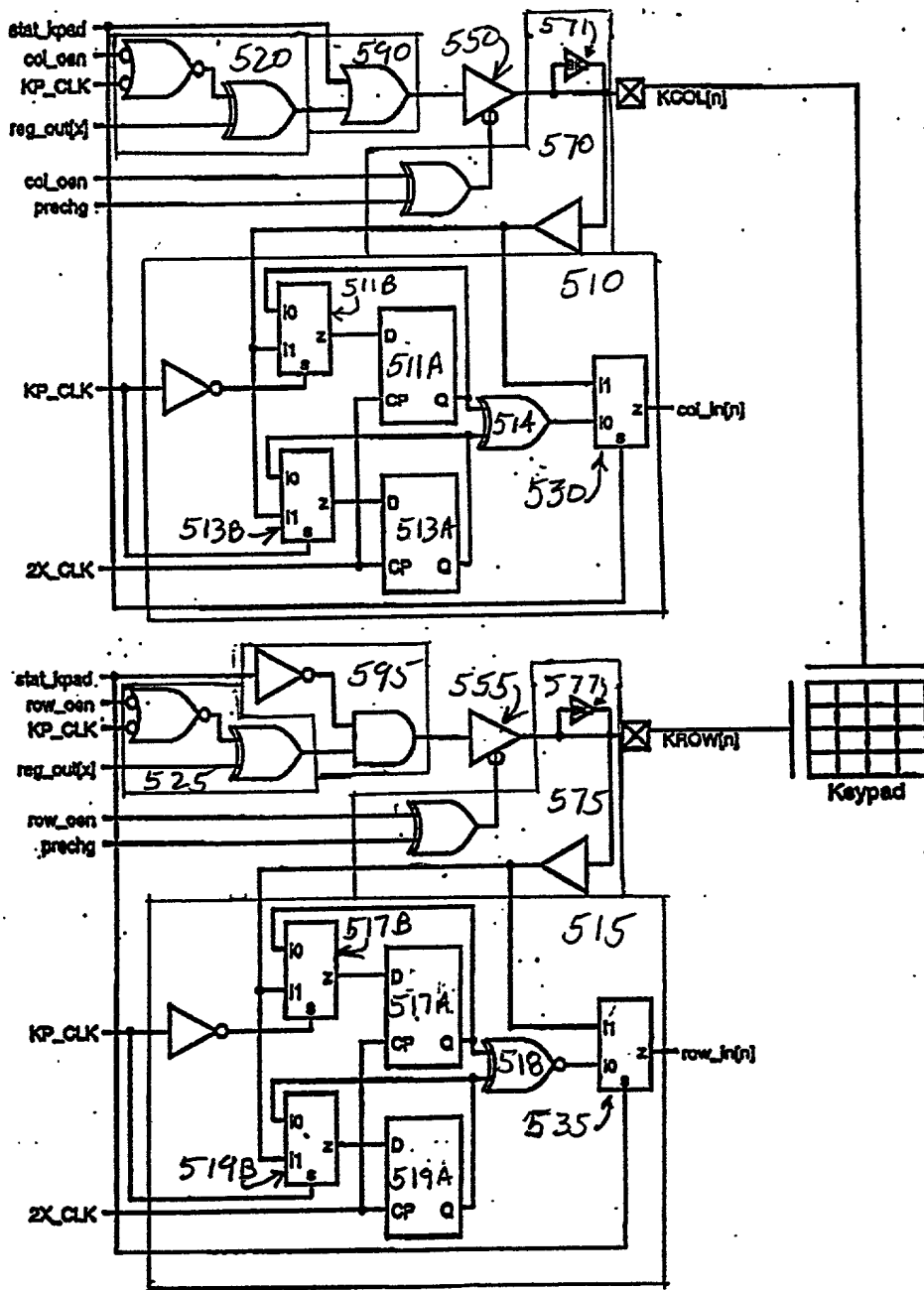


FIG 5

600

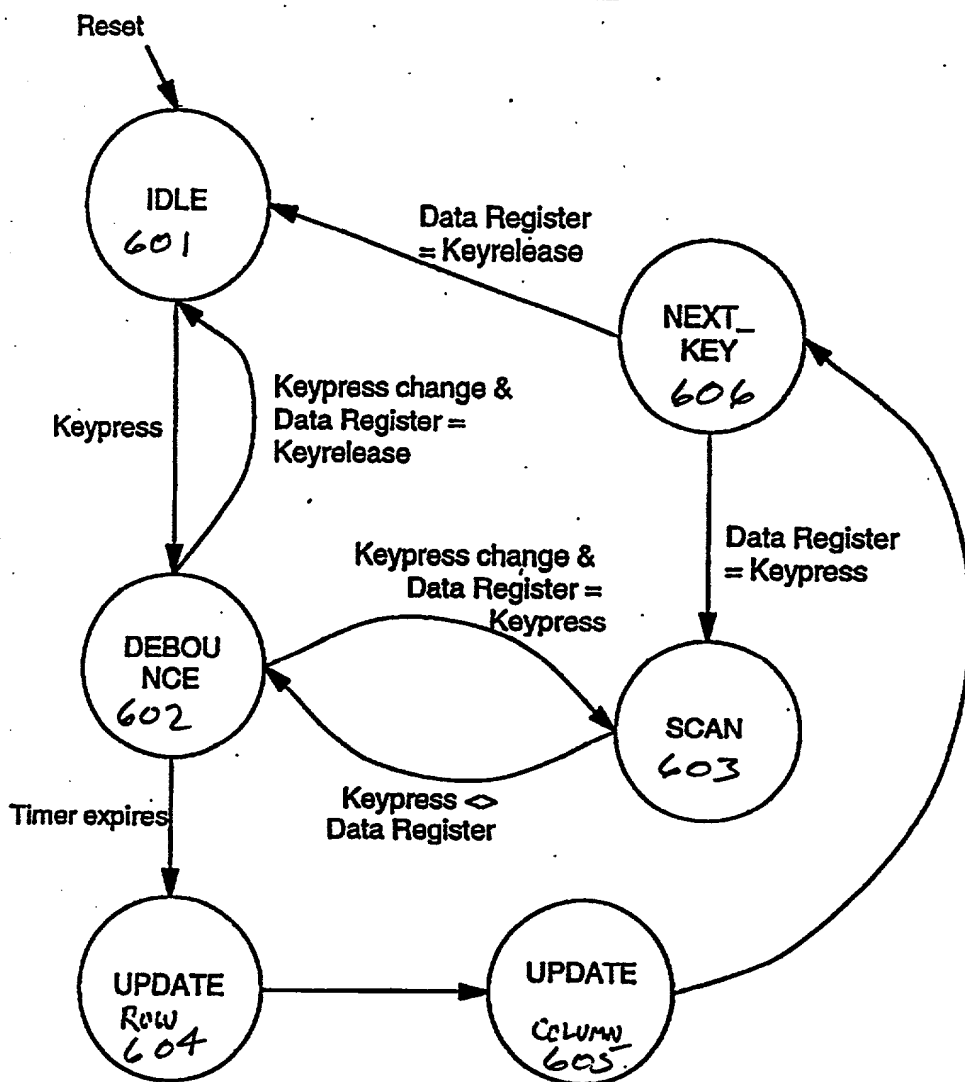


FIG 6A

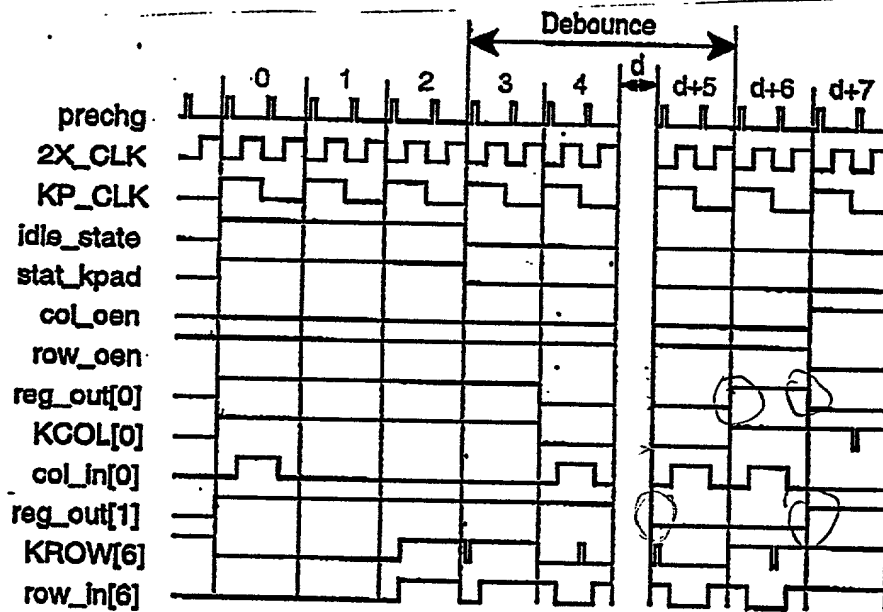


FIG 6B

VPB\_base+keyconfig+0h (04000000h+000xx000h+10h=040xx010h thru 040xx04Ch)

	D15	D14	D13	D12	D11	D10	D9	D8
	R							
POR	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	PAD_DRV							
POR	0	0	0	0	0	0	0	0

Bit	Name	Function
15:8	R	Reserved. These bits always return zero.
7:0	PAD_DRV	Pad drive data. Data driven out on either ROW[7:0] or COL[7:0]. The output (row or column) is driven with the data and the input (column or row) is pulled up or down, in the opposite direction of the data. 0 = drive the output low, pull up the input 1 = drive the output high, pull down the input

VPB\_base+keyconfig+0h (04000000h+000xx000h+50h=040xx050h)

	D15	D14	D13	D12	D11	D10	D9	D8
	LFSR_DATA[15:8]							
POR	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	LFSR_DATA[7:0]							
POR	0	0	0	0	0	0	0	1

Bit	Name	Function
7:0	LFSR_DATA	LFSR load data. This write only register provides parallel load data to the DATAIN connections of the LFSR.

FIG 7



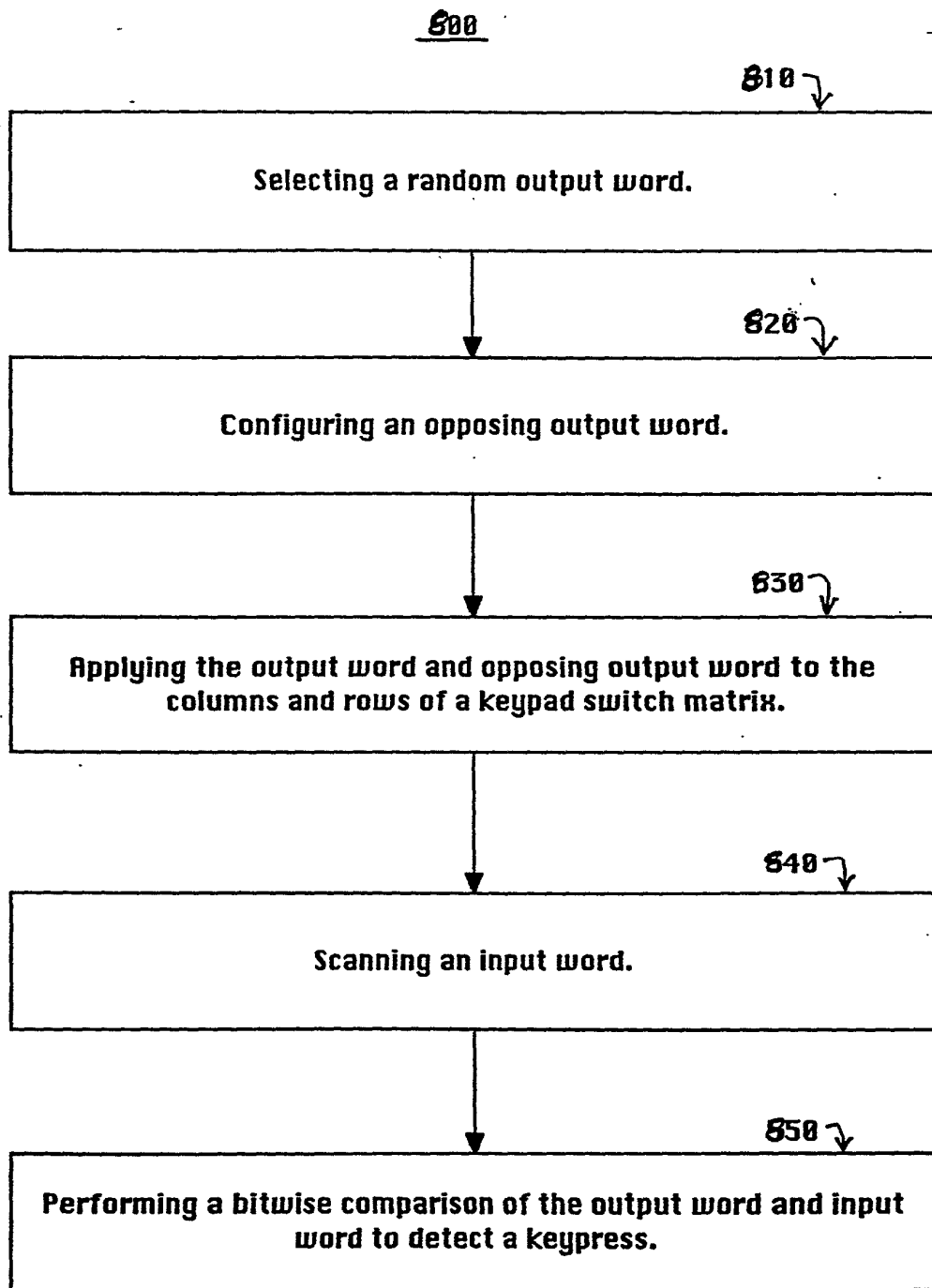


FIG 8